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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,135	11/10/1999	SHUNPEI YAMAZAKI	0756-2064	7576

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	28

DATE MAILED: 03/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/437,135	Applicant(s) YAMAZAKI ET AL.	
	Examiner Erik Kielin	Art Unit 2813	

-- Th MAILING DATE of this communication appears on th c v r she t with th correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 29-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 29-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,25* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action responds to IDS filed 10 November 1999 (Paper No 2), the IDS filed 6 November 2002 (Paper No. 25), and the Amendment filed 14 January 2003 (Paper No. 27).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-14 and 29-37 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Plasma CVD to deposit the insulating layer, critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Each of the independent claims 1, 6, 11, 30, and 34 has been amended to include that the limitation that the insulating film is formed by using TEOS at a temperature of 200 °C to 400 °C, for which Applicant has indicated that the specification provides support at p. 25, line 3 of the instant specification. (See Response by Applicant, Paper No. 27, p. 5, first full paragraph.) The specification, at the location indicated by Applicant, indicates that this method is a plasma CVD using RF power (specification, sentence bridging pp. 24-25). Moreover, Applicant indicates that deposition of SiO_2 from TEOS, as indicated in each of the Wolf and Roy references provided by Examiner, indicates that higher temperatures than 400 °C are required. (See Response by Applicant, Paper No. 27, p. 5, last paragraph through p. 6.) Accordingly, the evidence of record indicates that the insulating film could not be deposited using TEOS at 200 °C to 400 °C, absent

the critical limitation that the deposition method is plasma CVD, in accordance with Applicant's specification.

The remaining claims are rejected for depending from the above rejected claims.

3. Claims 3, 8, 13, 32, and 36 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Each of the aforementioned claims indicates that the insulating film deposition method is either low pressure CVD or plasma CVD. For the reasons just indicated, low pressure CVD would not work at 200 °C to 400 °C with TEOS as the SiO_2 precursor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **1**-4, **6**-9, **11**-13, 29, **30**-33, and **34**-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,274,279 (**Misawa** et al.) in view of Applicant's admitted prior art (**APA**), US 5,000,133 (**Wang** et al.), and the article **Ang** et al. "Electrical characterization of low-pressure chemical-vapor-deposited silicon dioxide metal-oxide-silicon structures" Journal of Applied Physics 73(5), 1 March 1993, pp. 2397-2401.

Regarding independent claims 1, 6, 11, 30, and 34, **Misawa** discloses a method of forming semiconductor devices, which are CMOS TFTs, comprising the steps of,

forming first, second, and third, patterned, crystallized col. 9, lines 19-26), silicon semiconductor islands **111**, **112**, **113** over a transparent substrate **110** (Figs. 4A; col. 7, lines 60-66);

forming gate insulating films **114**, **115**, **116** formed from silicon oxides (as further limited by instant claims 6 and 30; col. 6, lines 39-46) on each of the semiconductor islands using chemical vapor deposition (Fig. 4A; sentence bridging cols. 7-8);

forming gate electrodes **117**, **118**, **119** on each of the gate insulating films (Fig. 4A; sentence bridging cols. 7-8); and

introducing phosphorous into said first and second semiconductor islands and introducing boron into said second semiconductor island, wherein a dose amount of said boron is larger than that of said phosphorous (col. 8, lines 3-56 -- **especially lines 50-56**).

Misawa is silent to the method by which the semiconductor islands are formed but, as noted above, indicates that they are polycrystalline at col. 9, lines 19-26.

The **APA** discloses that it is known in the art to make a TFT by forming a semiconductor film comprising amorphous silicon over a substrate; crystallizing said semiconductor film by irradiating a laser light. (Applicant's specification, pages 2-4). It would have been obvious for one of ordinary skill in the art, at the time of the invention to apply the silicon islands **111**, **112**, **113** of **Misawa** by depositing amorphous silicon and laser crystallizing as taught by **APA**, because **Misawa** is silent to the method by which such polycrystalline patterned silicon islands are formed, such that one of ordinary skill would be motivated to use known methods for

forming such as that taught by **APA** to be known specifically for TFTs such as **Misawa** is making.

Then the only difference is that **Misawa** does not teach that the gate insulating layers of silicon oxides **114**, **115**, **116**, disclosed therein as deposited by CVD, are irradiated by an intense light, in an atmosphere comprising oxygen gas.

Ang teaches the benefits of depositing an insulating layer of SiO_2 for a gate oxide using CVD and then thermally annealing in oxygen using a Heatpulse 210T rapid thermal processor which emits high intensity IR light (instant claims 2, 7, 12, 31, and 35) (see attached document, page 1, from UC-Berkeley obtained by the Internet for verification) in order to reduce the interfacial layer density (called both "fixed charge density" and "interface state density" therein) to well below 10^{11} cm^{-2} (instant claims 4, 9, 29, 33, and 37). (See Abstract and section entitled "Experiment.") It would have been obvious to one of ordinary skill in the art at the time the invention was made to irradiate the gate insulating film **114**, **115**, **116** of **Misawa**, in accordance with the teaching in **Ang** for the numerous benefits taught by **Ang**, as just noted.

Finally, **Misawa** does not teach that the CVD method of forming the gate insulating layer silicon oxides **114**, **115**, **116** is deposited using TEOS at a temperature of 200 °C to 400 °C.

Wang teaches a method of forming conformal oxide layers for semiconductor fabrication wherein the conformal layer is deposited using plasma CVD with TEOS as the precursor gas at a temperature between 200 °C to 500 °C, preferably 375 °C ± 20 °C (col. 5, lines 11-31).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use plasma CVD ((instant claims 3, 8, 13, 32, and 36) with TEOS at 200 to 400 °C, as taught by **Wang**, to form the gate insulating film of **Misawa** because Misawa (1) is silent as to the exact

CVD method and (2) requires a conformal gate insulating film (Misawa Fig. 4A, **114**, **115**, **116**), such that one of ordinary skill would be motivated to use a known method that would give good conformal coverage, such as taught by **Wang**.

6. Claims 5, 10, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Misawa** in view of the **APA**, **Ang**, and **Wang** as applied to claims 1, 6, and 11 above, and further in view of **JP 60-187030**.

Misawa in view of the **APA** and **Ang** does not indicate the kind of laser to be used for crystallizing the silicon film.

JP 60187030 discloses the benefits of the instantly claimed excimer lasers for such crystallizing silicon (Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to crystallize the silicon using the lasers in **JP 60187030** for the reasons indicated therein and because excimer lasers are known for the purpose of crystallization of silicon films.

Response to Arguments

7. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The article **Jiang** et al. "Study of n-channel enhancement mode InP MISFETs" Chinese Journal of Semiconductors 9(5), September 1988, pp. 451-458, teaches plasma CVD of SiO_2 gate insulators using TEOS.

The article **Sun** et al. "High Quality MOSFET's with N2O Annealed Thin TEOS Gate Oxide" IEEE 1993 International Symposium on VLSI Technology, May 1993, pp. 109-111, teaches annealing CVD deposition of gate insulating films using TEOS followed by annealing in N_2O.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
March 17, 2003